AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1. (Previously Presented) A method for verifying a design of a circuit, comprising:

providing a model of the design;

providing a first property for the design, wherein the first property describes a first behavior;

checking the model using the first property and an environment of the design at a reset state until an example of the first behavior occurs;

providing a second property for the design, wherein the second property describes a second behavior; and

checking the model using the second property and an environment of the design at a state when the example of the first behavior occurs.

2. (Original) The method of claim 1, wherein providing the first property comprises:

providing a Boolean expression representing a formula that the first behavior does not occur, wherein the Boolean expression comprises a plurality of Boolean variables.

3. (Original) The method of claim 2, wherein checking the model using the first property comprises:

determining a set of values for the Boolean variables of the Boolean expression that causes the Boolean expression to be false.

4. (Original) The method of claim 1, further comprising:

providing the environment of the design at the reset state.

5. (Previously Presented) The method of claim 1, further comprising:

providing the environment of the design at the state when the example of the first behavior occurs.

6. (Original) The method of claim 5, wherein providing the environment of the design at the state when the example of the first behavior occurs comprises at least one of the group consisting of

describing the state when the example of the first behavior occurs; and providing the values of the Boolean variables of the Boolean expression.

7. (Currently Amended) A computer program stored on a computer-readable medium for use by a processor for verifying a design of a circuit, comprising:

providing a model of the design;

providing a first property for the design, wherein the first property describes a first behavior;

checking the model using the first property and an environment of the design at a reset state until an example of the first behavior occurs;

providing a second property for the design, wherein the second property describes a second behavior; and

checking the model using the second property and an environment of the design at a state when the example of the first behavior occurs.

8. (Original) The computer program of claim 7, wherein providing the first property comprises:

providing a Boolean expression representing a formula that the first behavior does not occur, wherein the Boolean expression comprises a plurality of Boolean variables.

9. (Original) The computer program of claim 8, wherein checking the model using the first property comprises:

determining a set of values for the Boolean variables of the Boolean expression that causes the Boolean expression to be false.

10. (Original) The computer program of claim 7, further comprising: providing the environment of the design at the reset state.

11. (Previously Presented) The computer program of claim 7, further comprising:

providing the environment of the design at the state when the example of the first behavior occurs.

12. (Original) The computer program of claim 11, wherein providing the environment of the design at the state when the example of the first behavior occurs comprises at least one of the group consisting of

describing the state when the example of the first behavior occurs; and providing the values of the Boolean variables of the Boolean expression.

13. (Currently Amended) ~~A semiconductor device~~ An electronic circuit verified by the method of claim 1.

14. (Currently Amended) ~~A semiconductor device~~ An electronic circuit verified by the computer program of claim 7.